Assignment No. 1

CMOS 2:1 Multiplexor using SPICE

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1. Introduction

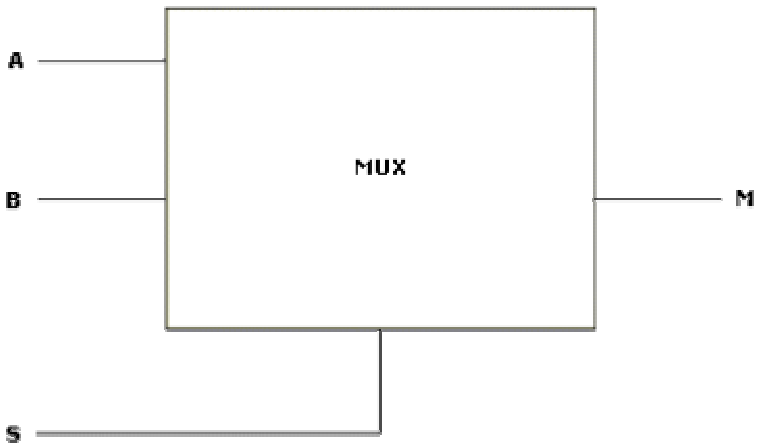
1. CMOS Multiplexor

The multiplexor is a very popular and most widely used combinational circuit. It has multiple inputs and one output. The input can be selected by a set of select lines. Multiplexors are key components in CMOS memory elements and data manipulation structures.

2. Block Diagram

CMOS 2:1 Multiplexor

The following figure shows the block diagram of full custom cell (CMOS) of 2 to 1 multiplexor. A 2 to 1 multiplexor has two inputs (A and B) and one select line(S). The circuit should select input A when S=0 and input B when S=1.



3 Functional Circuit

The truth table of 2:1 Multiplexor is shown below

A	B	S		M
0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		1
1	0	0		1
1	0	1		0
1	1	0		1
1	1	1		1

Karnaugh Map of 2:1 Multiplexor

S \ AB	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$\bar{M}=\bar{S}.\bar{A} + S.\bar{B}$

The decomposition of this expression and generation of the CMOS transistor circuit diagram is approached in following way:

i) For the n-side, take the un-inverted expression ($\bar{S}.\bar{A} + S.\bar{B}$); AND (.) operations are converted in series connection of NMOS while OR (+) operations are converted in parallel connection of NMOS.

For NMOS

$M=\overline{((\bar{S}.\bar{A}) + (S.\bar{B}))}$

ii) For the p-side invert the expression used for the n-expansion, yielding ($\bar{S}+\bar{A}$). ($S + \bar{B}$).(replacing AND with OR and vice-versa). OR (+)

operations are converted in parallel connection of PMOS while AND (.) operations are converted in series connection of PMOS.

For PMOS

M=¯ ((¯S+ ¯A). (S + ¯B))

iii) The final step requires connecting one end of the p-structure to '1' (VDD) and other to the output M. One side of the n-structure is connected to '0' (VSS) and other to the output in common with the PMOS.

This final diagram of multiplexor is yield below.

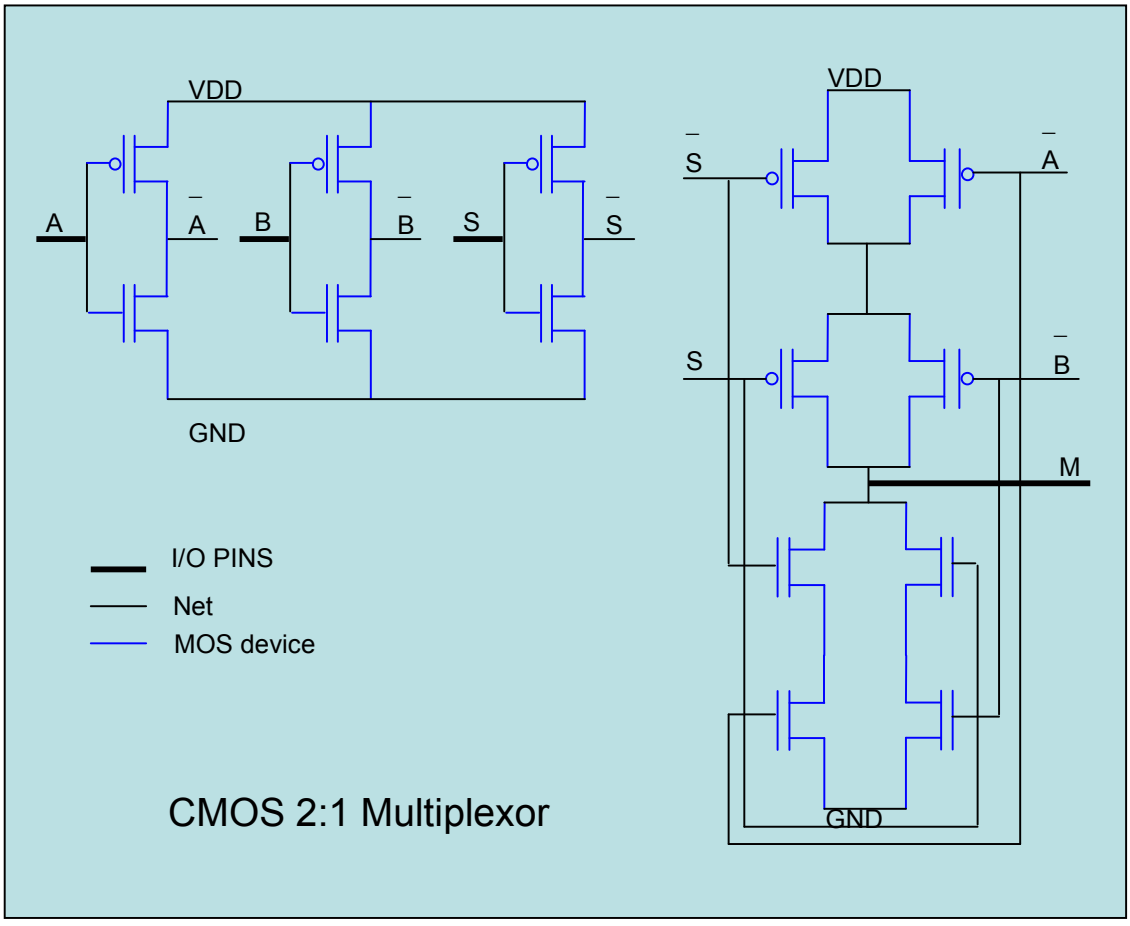


Fig. 1.3 CMOS 2:1 Multiplexor

4. Schematic

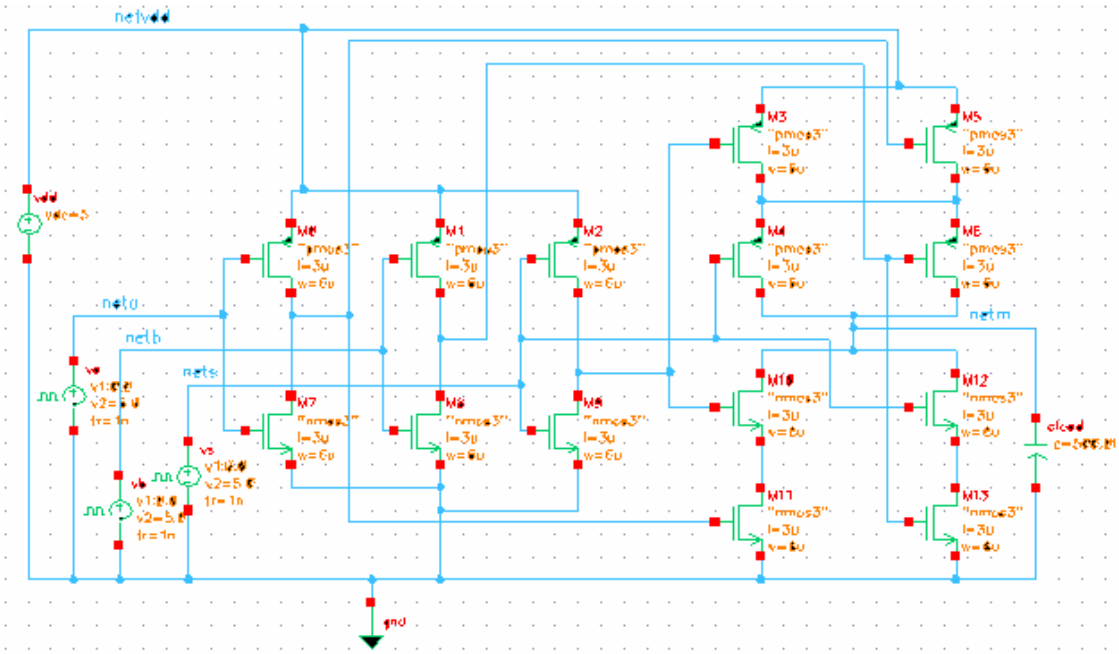


Fig. 1.4 Internal Schematic of Multiplexor cell

5. Circuit Simulation

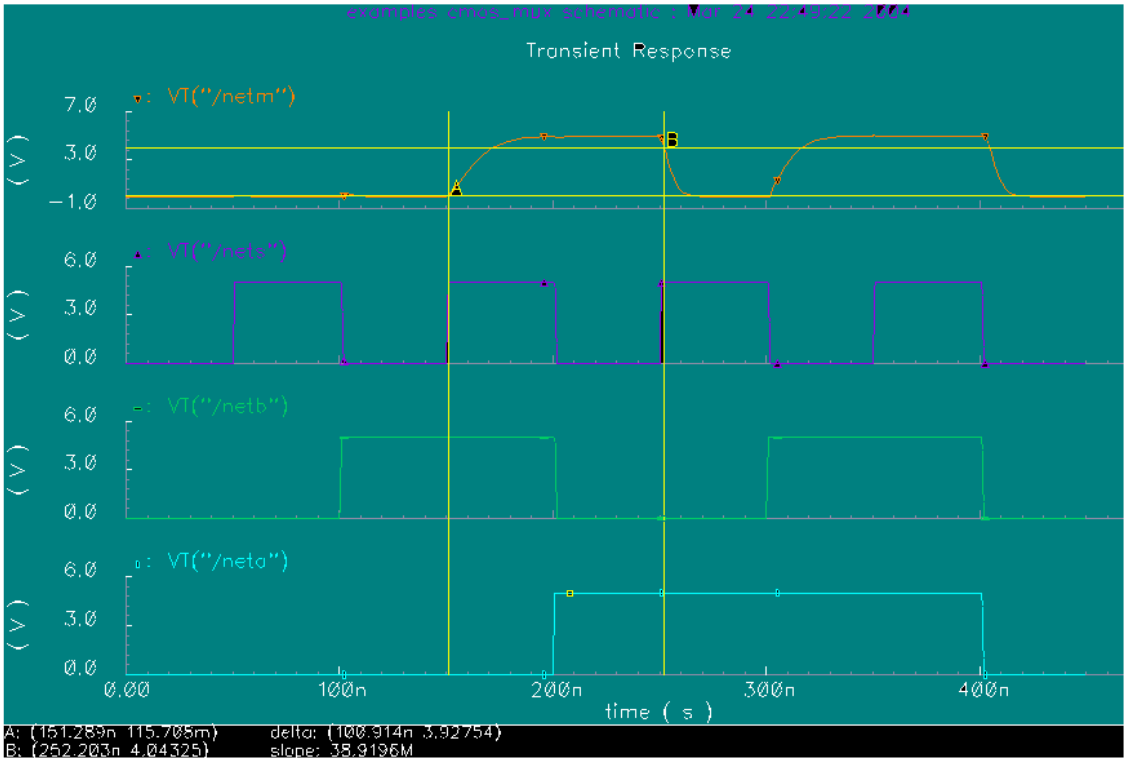


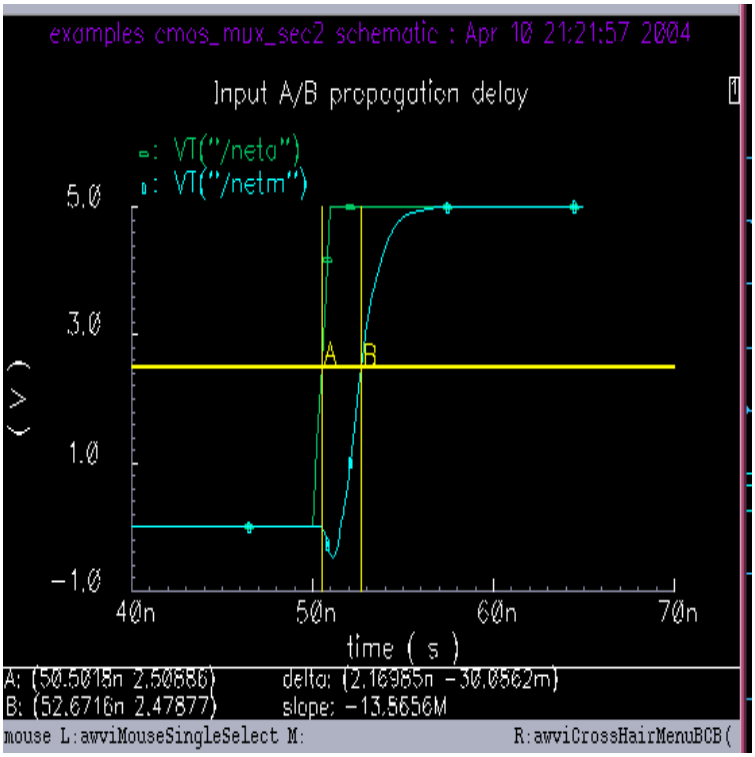
Fig.1.5 Transient Response of Input A, B, S and Output M.

Input A (neta - sky blue color)
Delay Time= 200ns
Pulse Width= 200ns
Period= 400ns

Input B (netb - green color)
Delay Time= 100ns
Pulse Width= 100ns
Period= 200ns

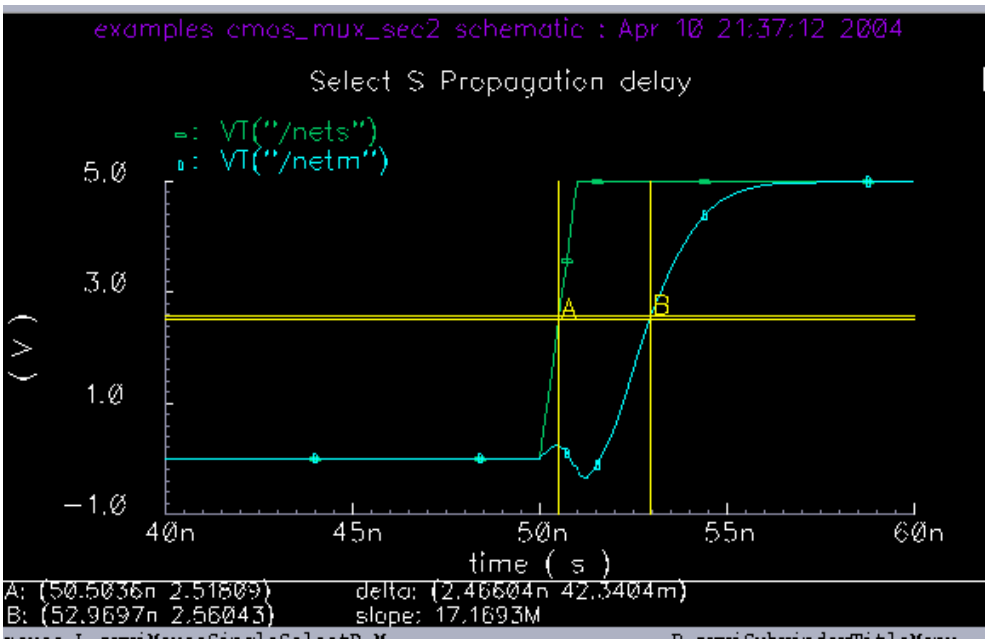
Input S (nets - blue color)
Delay Time= 50ns
Pulse Width= 50ns
Period= 100ns

Result Output (netm - yellow color)



Propagation delay a, b to m

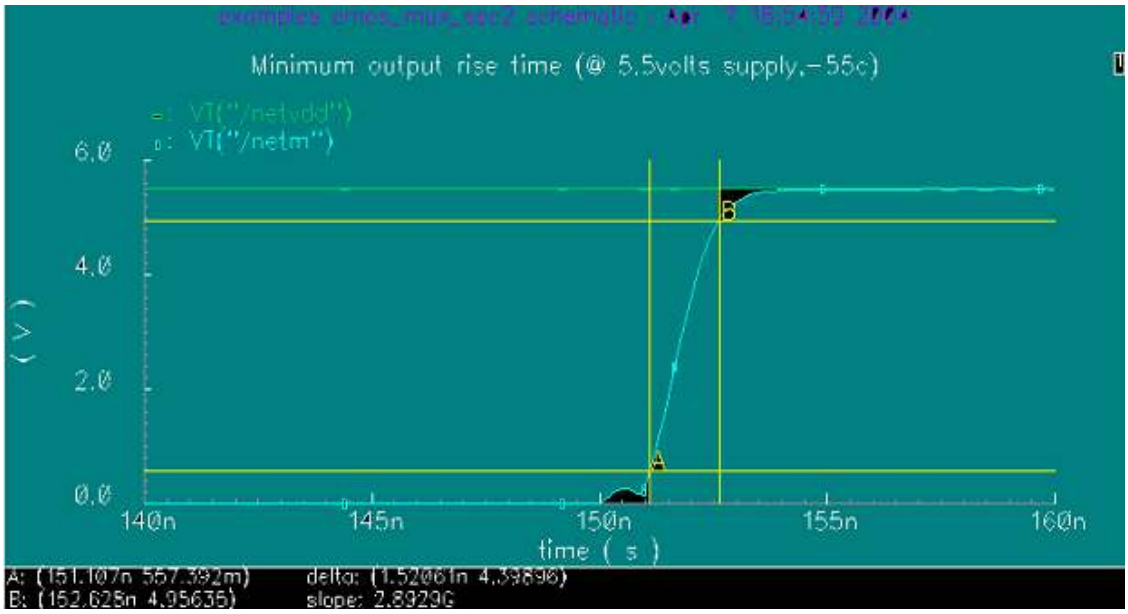
Propagation Delay



Propagation delay s to m

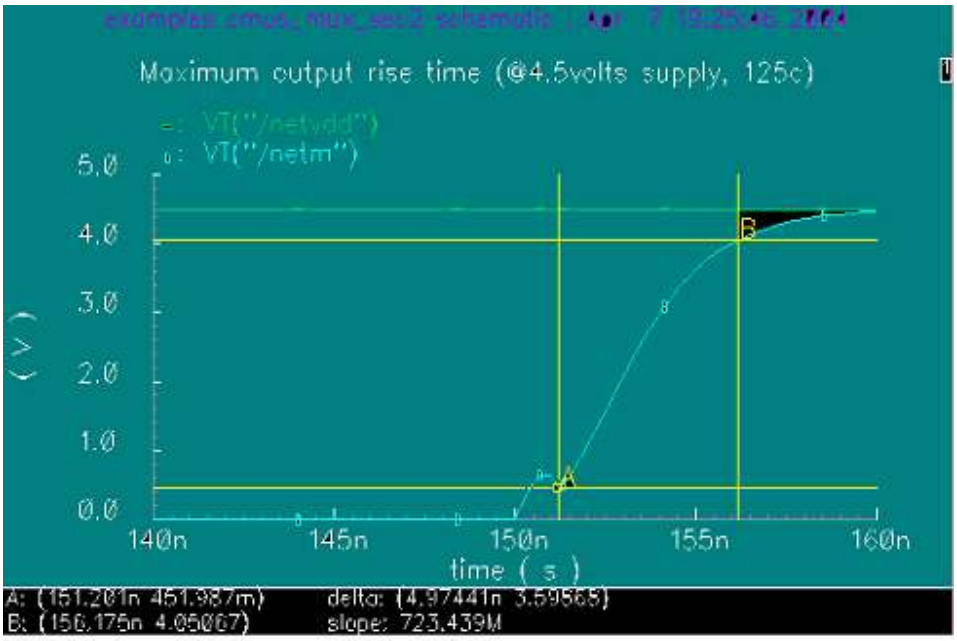
2. Parameters of the cell

Figure Number	Vdd	Temp (ºC)	Parameter	Description
2.1	5.5v	-55	$tr_{min} = 1.52ns$	Minimum output rise time
2.2	5.0v	25	$tr_{typ} = 2.75ns$	Typical output rise time
2.3	4.5v	125	$tr_{max} = 4.97ns$	Maximum output rise time
2.4	5.5v	-55	$tf_{min} = 0.53ns$	Minimum output fall time
2.5	5.0v	25	$tf_{typ} = 0.72ns$	Typical output fall time
2.6	4.5v	125	$tf_{max} = 1.14ns$	Maximum output fall time
2.7	5.0	25	$tr_{del} = 7.0ns$	Additional output rise time delay per unit load of 0.1pf
2.8	5.0	25	$tf_{del} = 2.35ns$	Additional output fall time delay per unit load of 0.1pf
2.9	5.5	-55	$I_{swmax} = 944uA$	Maximum switching current taken from the supply. (load=0.1pf)

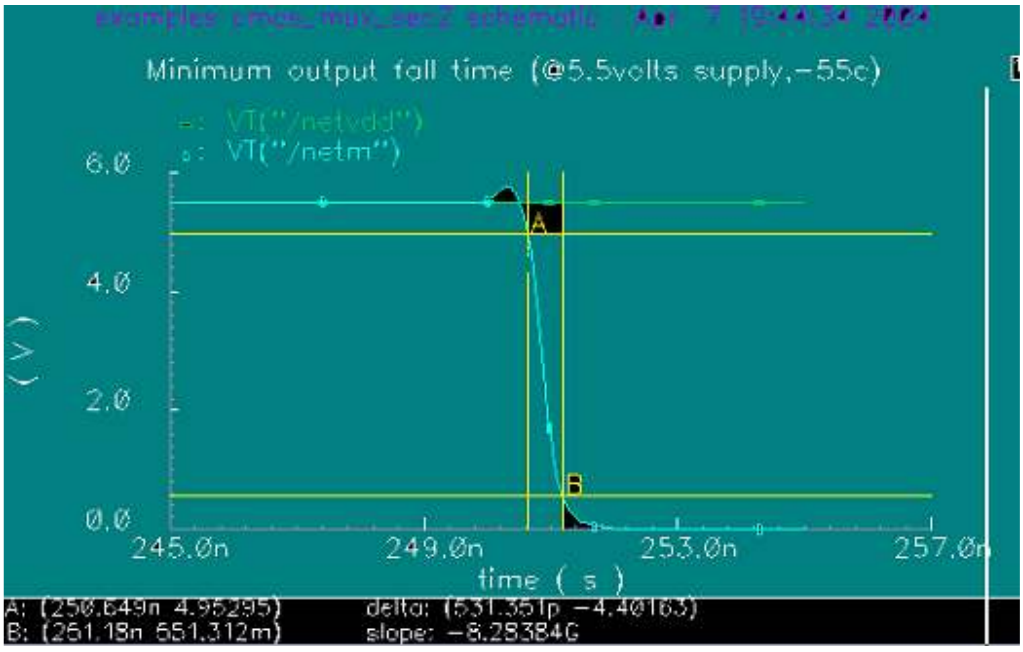


2.1 Minimum output rise time (1.52ns)

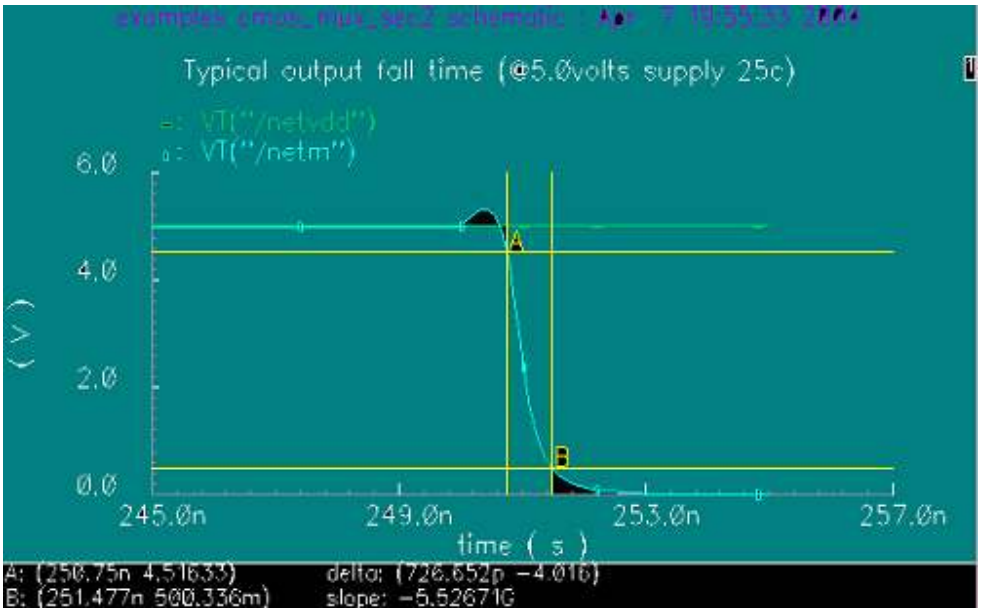
2.2 Typical output rise time (2.75ns)



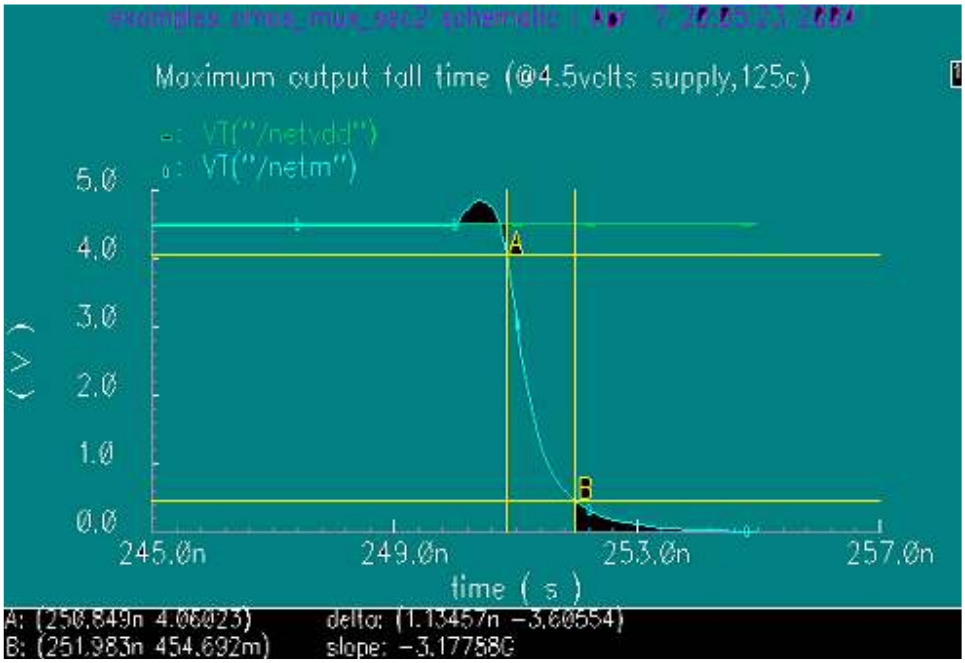
2.3 Maximum output rise time (4.97ns)



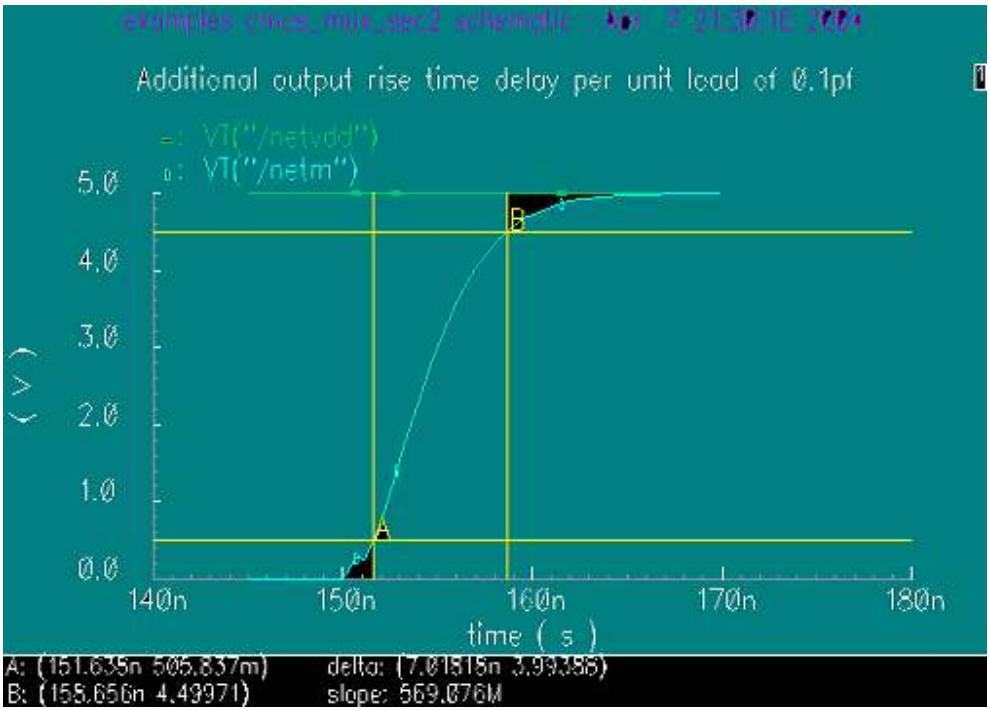
2.4 Minimum output fall time (0.53ns)



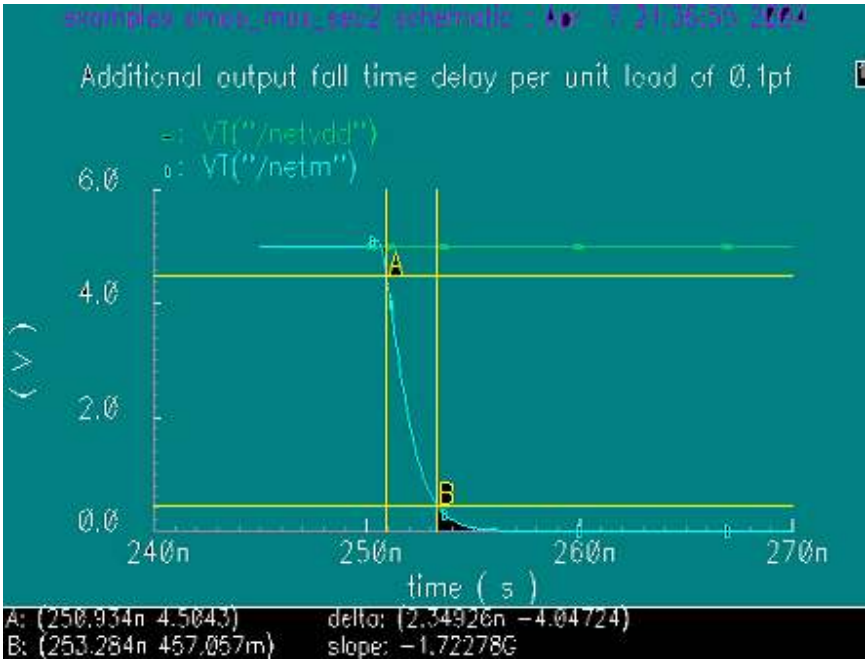
2.5 Typical output fall time (0.72ns)



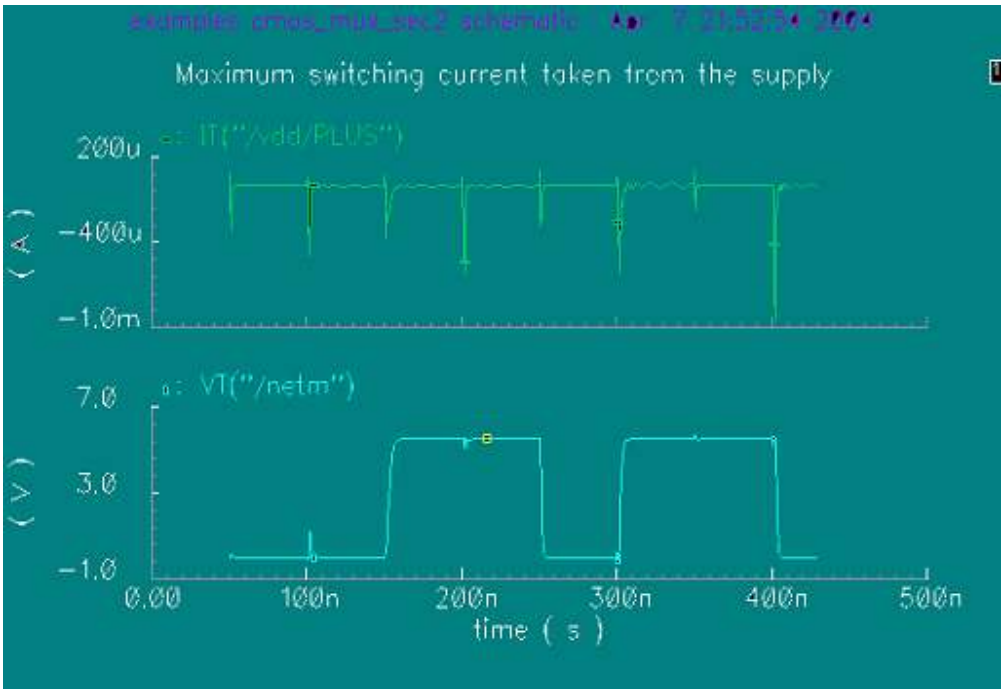
2.6 Maximum output fall time (1.14ns)



2.7 Additional output rise time delay per unit load of 0.1pf (7.0ns)



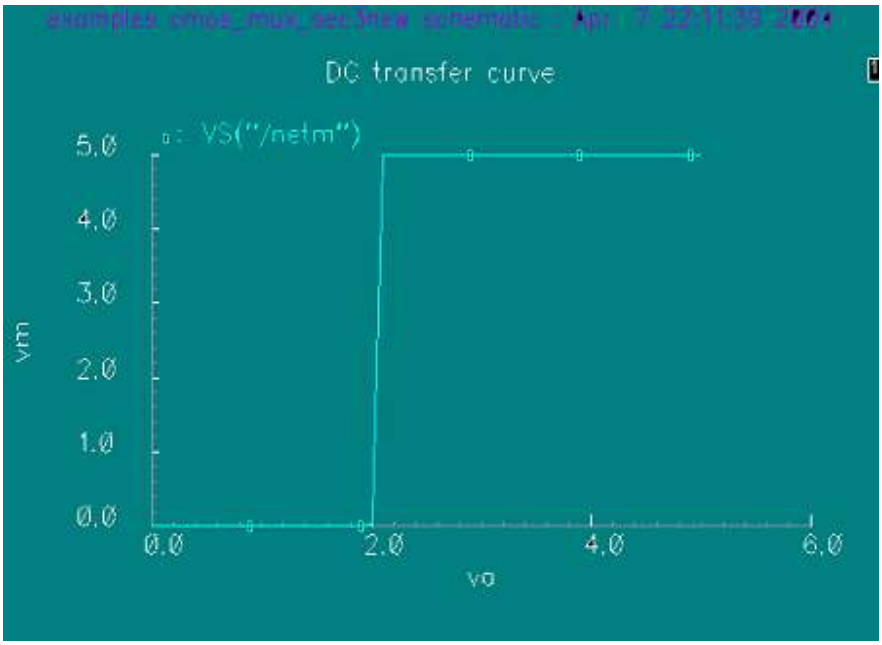
2.8 Additional output fall time delay per unit load of 0.1pf (2.35ns)



2.9 Maximum switching current taken from the supply (944uA)

3. DC transfer curve

Input B = 0v
S = 0v
Vcc = 5V, Temperature = 27ºC,
Load = 0.1pf.
Input A is swept from 0 to 5V while measuring output M.



DC transfer curve of va (input) VS vm (output)

FEATURES

- 5V tolerant inputs/outputs, for interfacing with 5V logic.
- Specified from -55 to 125 ºC
- Output drive capability 50 ohms transmission lines at 85 ºC
- CMOS power levels
- Resistor outputs (-15mA IOH, 12mA IOL)

Quick Reference Data
GND = 0V; tr = 2.75ns tf = 0.72ns; Tamb = 25 ºC

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
tPLH/tPHL	Propagation delay a, b to m	VDD= 5.0V unloaded	2.16	ns
	Propagation	VDD= 5.0V	2.46	ns

	delay s to m	unloaded		
CI	Input capacitance		0.01pF	pF
CPD	Power dissipation capacitance per gate	VDD = 5.0V	15.9 pF	pF

C_{IN} = Cgs + Cgd = (2eA)/ (3 tox) = 0.01pF
(e = 3.9 x 8.854 x 10 -14, tox = 200 °A A = W x L = 6u x 3u)
Cpd = I/(Vdd x Fi) – CL (eff)
= 800 uA/ (5 x 1/100ns) - 0.1pf
= 15.9 pF

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
VDD	Supply Voltage	for normal operation	4.5	5.5	V
Vi	Input voltage		0	5.5	V
Vo	Output voltage	High or Low state	0	VDD	V
Tamb	Operating ambient temperature	In free air	-55	+125	ºC
tr, tf	Input rise and fall times	VDD = 5.0V	0.72	2.75	ns

Pave = CL Vdd2 f where f = 1/T
= 0.1pF * 5.0 * 5.0 *(1/100ns)
= 25 uw
Psc = (β/12)(Vdd – 2Vt)3 (trf/tp)
(β = 30 uA/V2, Vdd = 5.0V Vt = , trf = 1ns, tp = 100ns)
= (2.5) (5-2) (0.03)
= 0.225 uw
where tp is the period of the input waveform and trf is the total risetime (or falltime)
tr = tf = trf

Ps = Σ 1-n Leakage current * suppy voltage (number of devices)
= Σ 1- 14 (0.2 nA * 5.0V)
= Σ 1- 14 (1nw)
= 14 nw

Ptotal = Pd + Psc + Ps

= 25uw + 0.225uw + 14nw
= 25.24uw
where Pd is the dynamic average power (previous chart), Psc is the short circuit power, and Ps is the static power due to ratio circuit current, junction leakage, and subthreshold Ioff leakage current

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	Test Conditions		MIN.	TYP.	MAX.	UNIT
		Other	VCC (V)				
Tamb = -55 to 125 ºC; note 1							
VIH	HIGH-level input voltage	Guaranteed Logic HIGH Level		2.8	-	-	V
VIL	LOW-level input voltage	Guaranteed Logic LOW Level		-	-	2.0	V
I_{IH}	Input HIGH Current(4)	V_I = 2.7V	V_{CC} = Max.	-	-		µA
I_{IL}	Input LOW Current(4)	V_I = 0.5V	V_{CC} = Max.	-	-		µA
I_I	Input HIGH Current(4)	V_I = V_{CC} (Max.)	V_{CC} = Max.	-	-		µA
VOH	HIGH-level output voltage	V_I = V_{IH} or V_{IL} I_O = –100 µA I_O = –12 mA I_O = –18 mA I_O = –24 mA	V_{CC} = Min	4.8			V
VOL	LOW- level output voltage	V_I = V_{IH} or V_{IL} I_O = 100 µA I_O = 12 mA I_O = 24 mA	V_{CC} = Min	0.1			V
ILI	Input leakage current	V_I = 5.5 V or GND					µA
IOZ	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND					µA
IOFF	Power-off leakage supply	V_I or V_O = 5.5 V					µA
ICC	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	V_{CC} = Max.	-			µA
ΔIcc	Additional quiescent supply	V_I = V_{CC} – 0.6 V; I_O = 0	V_{CC} = Max.				µA

	current per pin						

Notes

1. All typical values are measured Tamb = 25 ºC

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)				-	
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)				-	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5∝A at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		-			mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open OE = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND				
I_C Total Power Supply Current(6)		V_{CC} = Max. Outputs Open fo = 10MHz	V_{IN} = V_{CC} V_{IN} = GND				
		50% Duty	V_{IN} = 3.4V	-			

		Cycle OE = GND VIN = GND One Bit Toggling					
		VCC = Max. Outputs Open fo = 2.5MHz 50% Duty Cycle OE = GND Four Bits Toggling	VIN = VCC VIN = GND VIN = 3.4V VIN = GND				

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient.
3. Per TTL driven input (VIN = 3.4V). All other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of □ICC formula. These limits are guaranteed but not tested.
6. IC = IQUIESCENT + IINPUTS + IDYNAMIC
IC = ICC + □ICC DHNT + ICCD (fONO)
ICC = Quiescent Current
□ICC = Power Supply Current for a TTL High Input (VIN = 3.4V)
DH = Duty Cycle for TTL Inputs High
NT = Number of TTL Inputs at DH
ICCD = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
fO = Output Frequency
NO = Number of Outputs at fO
All currents are in milliamps and all frequencies are in megahertz.

CAPACITANCE (Ta = +25 ºC, F = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

Applications
Digital Multiplexing
Signal Gating